1.(amended) A semiconductor integrated circuit comprising:

contact pads positioned over active components, said contact pads stress-absorbing; and

at least one metallization layer between said contact pads and said active components, said metallization layer patterned and vertically coupled upward to said contact pads and vertically coupled downward to said active components.

3.(amended) A semiconductor integrated circuit comprising:

contact pads located over active components and including electro-plated portions; and

at least one metallization layer between said contact pads and said active components, said metallization layer patterned and vertically coupled upward to said contact pads and vertically coupled downward to said active components.

5.(amended) A semiconductor integrated circuit comprising:

a laterally organized power transistor;

an array of power supply contact pads distributed over said power transistor, said contact pads characterized by multiple metal layers including at least one electro-plated layer;

means for providing a distributed, predominantly vertical current flow from said contact pads to said transistor; and

means for connecting a power source to each of said contact pads.

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1.(amended) A semiconductor integrated circuit comprising:

contact pads ~~located~~ positioned over active components, said contact pads stress-absorbing; and

~~the position of said pads selected to provide control and distribution of power to said active components below said pads.~~

at least one metallization layer between said contact pads and said active components, said metallization layer patterned and vertically coupled upward to said contact pads and vertically coupled downward to said active components.

3.(amended) A semiconductor integrated circuit comprising:

contact pads located over active components and including electro-plated portions; and

~~said pads positioned to minimize the distance for power delivery between a selected pad and one or more corresponding active components, to which said power is to be delivered.~~

at least one metallization layer between said contact pads and said active components, said metallization layer patterned and vertically coupled upward to said contact pads and vertically coupled downward to said active components.

Delete claim 4.

5.(amended) A semiconductor integrated circuit comprising:

a laterally organized power transistor;

an array of power supply contact pads distributed over said power transistor, said contact pads characterized by multiple metal layers including at least one electro-plated layer;

means for providing a distributed, predominantly vertical current flow from said contact pads to said transistor; and

means for connecting a power source to each of said contact pads.

Applicants reply that amended claim 5 requires the contact pads include an electro-plated layer; whereas, Sato makes the contact pad from the same structure as the other metallization layer (e.g., Fig.19 discussion).

Respectfully submitted,

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